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Z86E33/733/E34
Z86E43/743/E44

CMOS Z8® OTP MICROCONTROLLERS

FEATURES

Device	ROM (KBytes)	RAM* (Bytes)	I/O Lines	Speed (MHz)
Z86E33	4	237	24	16
Z86733	8	237	24	16
Z86E34	16	237	24	16
Z86E43	4	236	32	16
Z86743	8	236	32	16
Z86E44	16	236	32	16

Note: *General-Purpose

- Standard Temperature (V_{CC} = 3.5V to 5.5V)
- Extended Temperature (V_{CC} = 4.5V to 5.5V)
- 28-Pin DIP/SOIC/PLCC Packages (E33/733/E34)
  40-Pin DIP Package (E43/743/E44)
  44-Pin PLCC/QFP Packages (E43/743/E44)
- Software Enabled Watch-Dog Timer (WDT)
- Push-Pull/Open-Drain Programmable on Port 0, Port 1, and Port 2
- Low-Power Consumption: 60 mW
- Programmable Crystal Oscillator, EPROM Protect, RAM Protect, Auto Latch Disable, Permanent WDT, 32 KHz Oscillator, and EPROM /Test Mode Disable
- Fast Instruction Pointer: 0.6µs
- Two Standby Modes: STOP and HALT
- 24/32 Input and Output Lines
- Digital Inputs CMOS Levels, Schmitt-Triggered
- Software Programmable Low EMI Mode
- Two Programmable 8-Bit Counter/Timers Each with a 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- Auto Latches
- Auto Power-On Reset (POR)
- Two Comparators
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive

GENERAL DESCRIPTION

The Z86E33/733/E34/E43/743/E44 8-bit CMOS One-Time Programmable (OTP) microcontrollers are members of Zilog's Z8® single-chip microcontroller family featuring enhanced wake-up circuitry, programmable Watch-Dog Timers, Low Noise EMI options, and easy hardware/software system expansion capability.

Four basic address spaces support a wide range of memory configurations. The designer has easy access to register mapped peripheral and I/O circuits.

For applications demanding powerful I/O capabilities, the Z86E33/733/E34 have 24 pins and the Z86E43/743/E44 have 32 pins of dedicated input and output. These lines are grouped into four ports, eight lines per port, and are configurable under software control to provide timing, status signals, and parallel I/O with or without handshake, and address/data bus for interfacing external memory.

Notes: All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

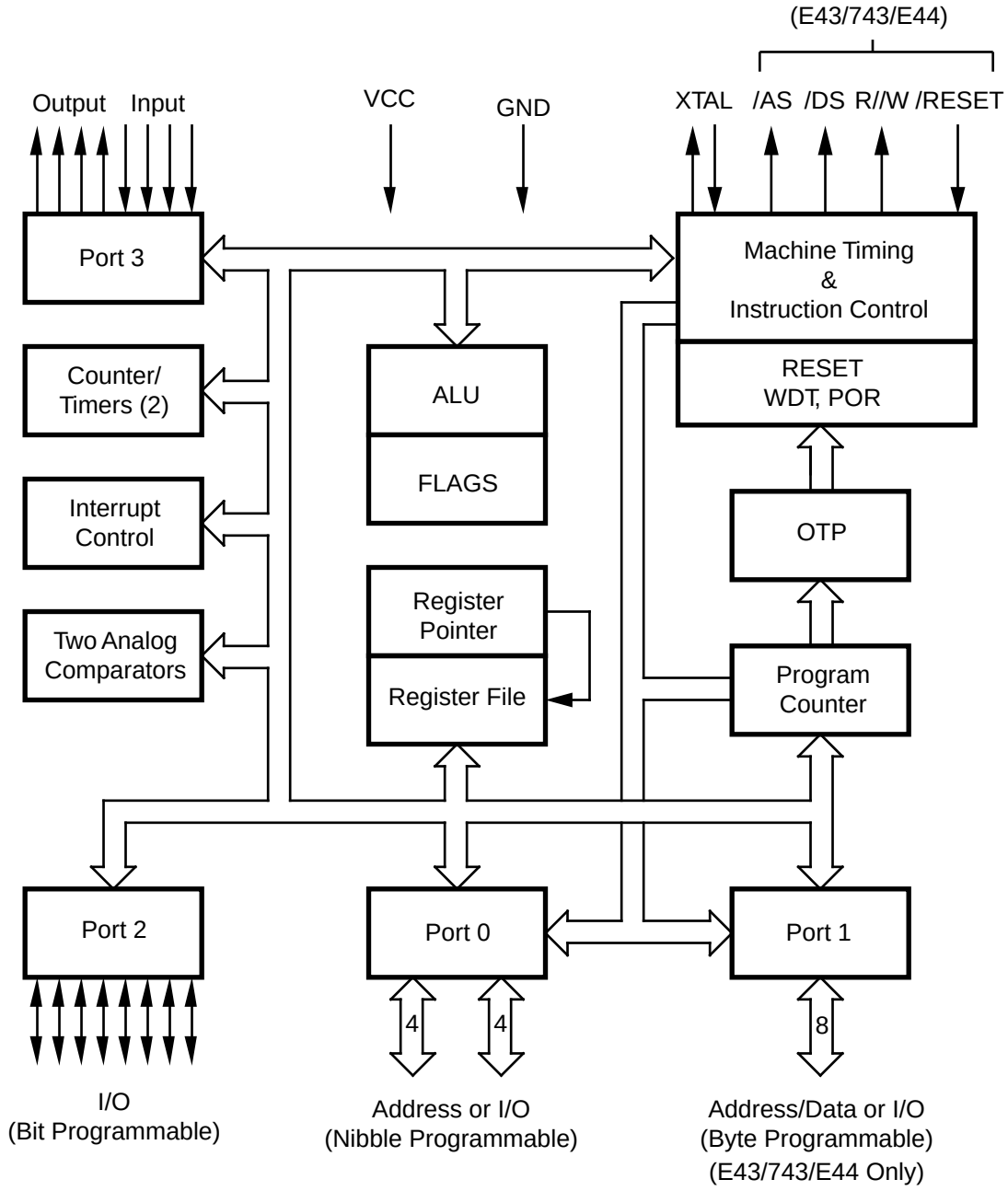

Figure 1. Functional Block Diagram

PIN IDENTIFICATION

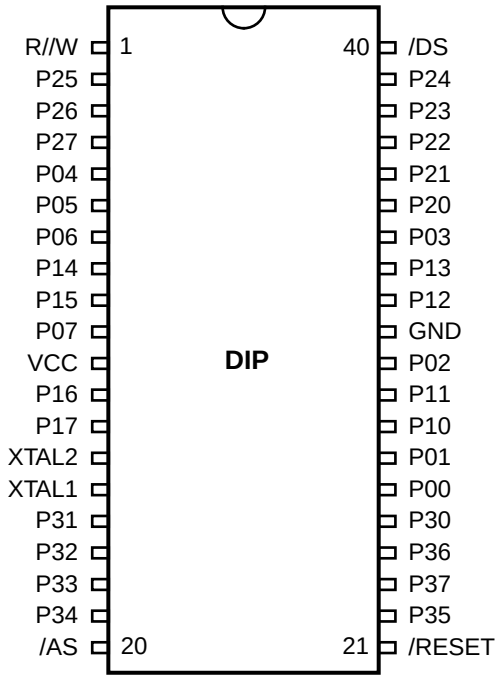

Figure 2. 40-Pin DIP Pin Configuration Standard Mode

Table 1. 40-Pin DIP Pin Identification Standard Mode

Pin #	Symbol	Function	Direction
1	R//W	Read/Write	Output
2-4	P25-P27	Port 2, Pins 5,6,7	In/Output
5-7	P04-P06	Port 0, Pins 4,5,6	In/Output
8-9	P14-P15	Port 1, Pins 4,5	In/Output
10	P07	Port 0, Pin 7	In/Output
11	V_{CC}	Power Supply	
12-13	P16-P17	Port 1, Pins 6,7	In/Output
14	XTAL2	Crystal Oscillator	Output
15	XTAL1	Crystal Oscillator	Input
16-18	P31-P33	Port 3, Pins 1,2,3	Input
19	P34	Port 3, Pin 4	Output
20	/AS	Address Strobe	Output
21	/RESET	Reset	Input
22	P35	Port 3, Pin 5	Output
23	P37	Port 3, Pin 7	Output
24	P36	Port 3, Pin 6	Output
25	P30	Port 3, Pin 0	Input
26-27	P00-P01	Port 0, Pins 0,1	In/Output
28-29	P10-P11	Port 1, Pins 0,1	In/Output
30	P02	Port 0, Pin 2	In/Output
31	GND	Ground	
32-33	P12-P13	Port 1, Pins 2,3	In/Output
34	P03	Port 0, Pin 3	In/Output
35-39	P20-P24	Port 2, Pins 0,1,2,3,4	In/Output
40	DS	Data Strobe	Output

Notes:
Pin Configuration and Identification identical on DIP and Cerdip Window Lid style packages.

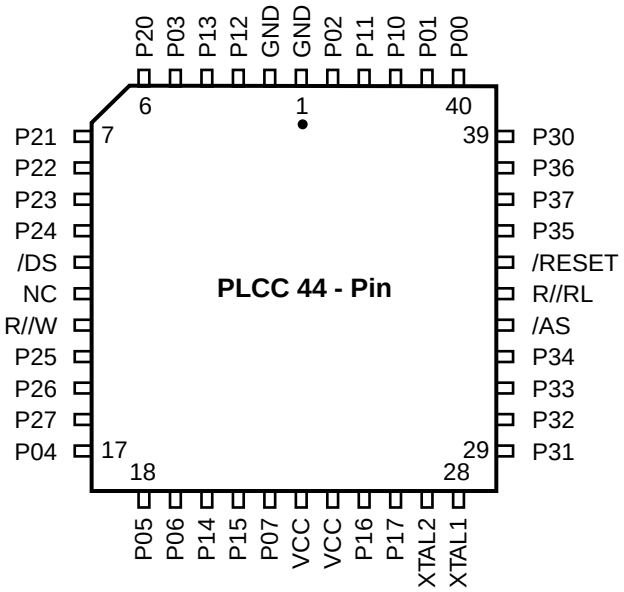

Figure 3. 44-Pin PLCC Pin Configuration
Standard Mode

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1-2	GND	Ground	
3-4	P12-P13	Port 1, Pins 2,3	In/Output
5	P03	Port 0, Pin 3	In/Output
6-10	P20-P24	Port 2, Pins 0,1,2,3,4	In/Output
11	/DS	Data Strobe	Output
12	NC	No Connection	
13	R//W	Read/Write	Output
14-16	P25-P27	Port 2, Pins 5,6,7	In/Output
17-19	P04-P06	Port 0, Pins 4,5,6	In/Output
20-21	P14-P05	Port 1, Pins 4,5	In/Output
22	P07	Port 0, Pin 7	In/Output
23-24	VCC	Power Supply	
25-26	P16-P17	Port 1, Pins 6,7	In/Output
27	XTAL2	Crystal Oscillator	Output
28	XTAL1	Crystal Oscillator	Input
29-31	P31-P33	Port 3, Pins 1,2,3	Input
32	P34	Port 3, Pin 4	Output

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
33	/AS	Address Strobe	Output
34	R//RL	ROM/ROMless select	Input
35	/RESET	Reset	Input
36	P35	Port 3, Pin 5	Output
37	P37	Port 3, Pin 7	Output
38	P36	Port 3, Pin 6	Output
39	P30	Port 3, Pin 0	Input
40-41	P00-P01	Port 0, Pins 0,1	In/Output
42-43	P10-P11	Port 1, Pins 0,1	In/Output
44	P02	Port 0, Pin 2	In/Output

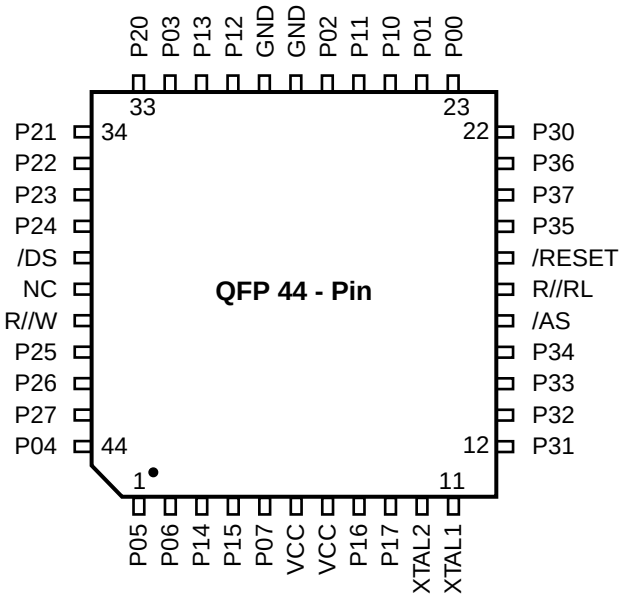

Figure 4. 44-Pin QFP Pin Configuration
Standard Mode

Table 3. 44-Pin QFP Pin Identification

Pin #	Symbol	Function	Direction
1-2	P05-P06	Port 0, Pins 5,6	In/Output
3-4	P14-P05	Port 1, Pins 4,5	In/Output
5	P07	Port 0, Pin 7	In/Output
6-7	VCC	Power Supply	
8-9	P16-P17	Port 1, Pins 6,7	In/Output
10	XTAL2	Crystal Oscillator	Output
11	XTAL1	Crystal Oscillator	Input
12-14	P31-P13	Port 3, Pins 1,2,3	Input
15	P34	Port 3, Pin 4	Output
16	/AS	Address Strobe	Output
17	R//RL	ROM/ROMless select	Input
18	/RESET	Reset	Input
19	P35	Port 3, Pin 5	Output
20	P37	Port 3, Pin 7	Output
21	P36	Port 3, Pin 6	Output
22	P30	Port 3, Pin 0	Input
23-24	P00-P01	Port 0, Pins 0,1	In/Output
25-26	P10-P11	Port 1, Pins 0,1	In/Output

Table 3. 44-Pin QFP Pin Identification

Pin #	Symbol	Function	Direction
27	P02	Port 0, Pin 2	In/Output
28-29	GND	Ground	
30-31	P12-P13	Port 1, Pins 2,3	In/Output
32	P03	Port 0, Pin 3	In/Output
33-37	P20-4	Port 2, Pins 0,1,2,3,4	In/Output
38	/DS	Data Strobe	Output
39	NC	No Connection	
40	R//W	Read/Write	Output
41-43	P25-P27	Port 2, Pins 5,6,7	In/Output
44	P04	Port 0, Pin 4	In/Output

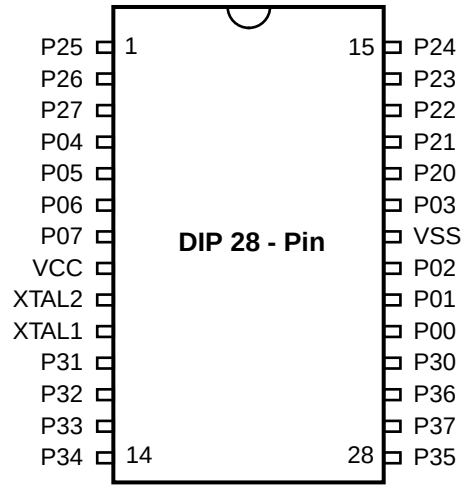

Figure 5. Standard Mode 28-Pin DIP/SOIC Pin Configuration

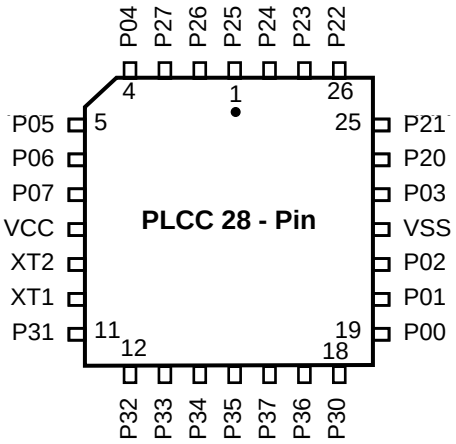

Figure 6. Standard Mode 28-Pin PLCC Pin Configuration

Table 4. 28-Pin DIP/SOIC/PLCC Pin Identification

Pin #	Symbol	Function	Direction
1-3	P25-P27	Port 2, Pins 5,6,7	In/Output
4-7	P04-P07	Port 0, Pins 4,5,6,7	In/Output
8	V_{CC}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11-13	P31-P33	Port 3, Pins 1,2,3	Input
14-15	P34-P35	Port 3, Pins 4,5	Output
16	P37	Port 3, Pin 7	Output
17	P36	Port 3, Pin 6	Output
18	P30	Port 3, Pin 0	Input
19-21	P00-P02	Port 0, Pins 0,1,2	In/Output
22	V_{SS}	Ground	
23	P03	Port 0, Pin 3	In/Output
24-28	P20-P24	Port 2, Pins 0,1,2,3,4	In/Output

Notes:
Pin Identification and Configuration identical on DIP and Cerdip Window Lid style packages.

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Ambient Temperature under Bias	–40	+105	C
Storage Temperature	–65	+150	C
Voltage on any Pin with Respect to V_{SS} [Note 1]	–0.6	+7	V
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V
Voltage on XTAL1 and /RESET Pins with Respect to V_{SS} [Note 2]	–0.6	V_{DD}+1	V
Total Power Dissipation		1.21	W
Maximum Allowable Current out of V_{SS}		220	mA
Maximum Allowable Current into V_{DD}		180	mA
Maximum Allowable Current into an Input Pin [Note 3]	–600	+600	µA
Maximum Allowable Current into an Open-Drain Pin [Note 4]	–600	+600	µA
Maximum Allowable Output Current Sinked by Any I/O Pin		25	mA
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA

Notes:
1. This applies to all pins except XTAL pins and where otherwise noted.
2. There is no input protection diode from pin to V_{DD}.
3. This excludes XTAL pins.
4. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Total power dissipation should not exceed 1.2 W for the package. Power dissipation is calculated as follows:

Total Power Dissipation = V_{DD} x [I_{DD} – (sum of I_{OH})]
+ sum of [(V_{DD} – V_{OH}) x I_{OH}]
+ sum of (V_{0L} x I_{0L})

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Test Load).

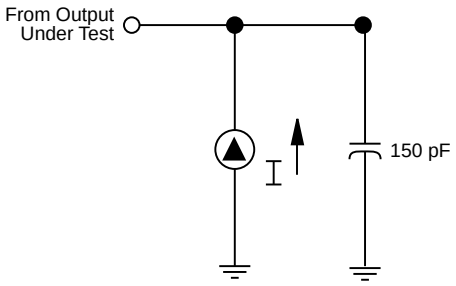

Figure 7. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz; unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

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